Application Note 66
Watchdog Timekeeper

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GENERAL OVERVIEW

Many applications require a real time clock to keep track of absolute time. Often these same applications could benefit by being told to perform certain functions at specific times. The Watchdog Timekeeper family from Dallas Semiconductor is a solution to systems that need both an accurate real time clock and interrupt capabilities at specific times. In addition, the Dallas Watchdog Timekeeper family provides an upgradeable nonvolatile RAM path.

Dallas Watchdog Timekeepers provide basic real time clock functions. The devices keep track of hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The time is accurately maintained by a very low power oscillator. The Watchdog Timekeeper modules, which contain the Watchdog integrated circuit as well as a crystal and lithium battery, provide an accuracy of ±1 minute per month. Because of the low power oscillator, the internal lithium battery provides 10 years of continuous operation in the absence of system power.

The Dallas Watchdog Timekeeper family is made up of the DS1283 and DS1284 integrated circuits as well as the DS1286, DS1386, and DS1486 modules. Table 1 lists the different devices that belong to this family. As can be seen in the table, this family provides an upgradeable nonvolatile RAM growth path.

THE DALLAS WATCHDOG TIMEKEEPER FAMILY Table 1

DEVICE	NVRAM	
DS1283	50 bytes	IC
DS1284	50 bytes	IC
DS1286	50 bytes	Module
DS1386-08	8K bytes	Module
DS1386-32	32K bytes	Module
DS1486	128K bytes	Module

One benefit of using Dallas Watchdog Timekeepers is that the devices are simple to use since the real time clock registers are mapped directly into the device's onboard RAM. This makes accessing the timekeeping registers analogous to accessing a byte in RAM. See Figure 1 for the memory map of the DS1486, for example. Note that the real time clock registers occupy only the top 14 bytes of the memory.

An additional benefit that simplifies the design effort when using the Watchdog family is that the DS1386 and DS1486 pinouts are very close to the standard JEDEC bytewide pinout for SRAMs. The two interrupt outputs and the square wave output are the only pins that differ from the JEDEC pinout. See Figure 2 for a comparison of standard JEDEC bytewide pinouts compared to the pinouts of the DS1386 and the DS1486.

INTERRUPTS

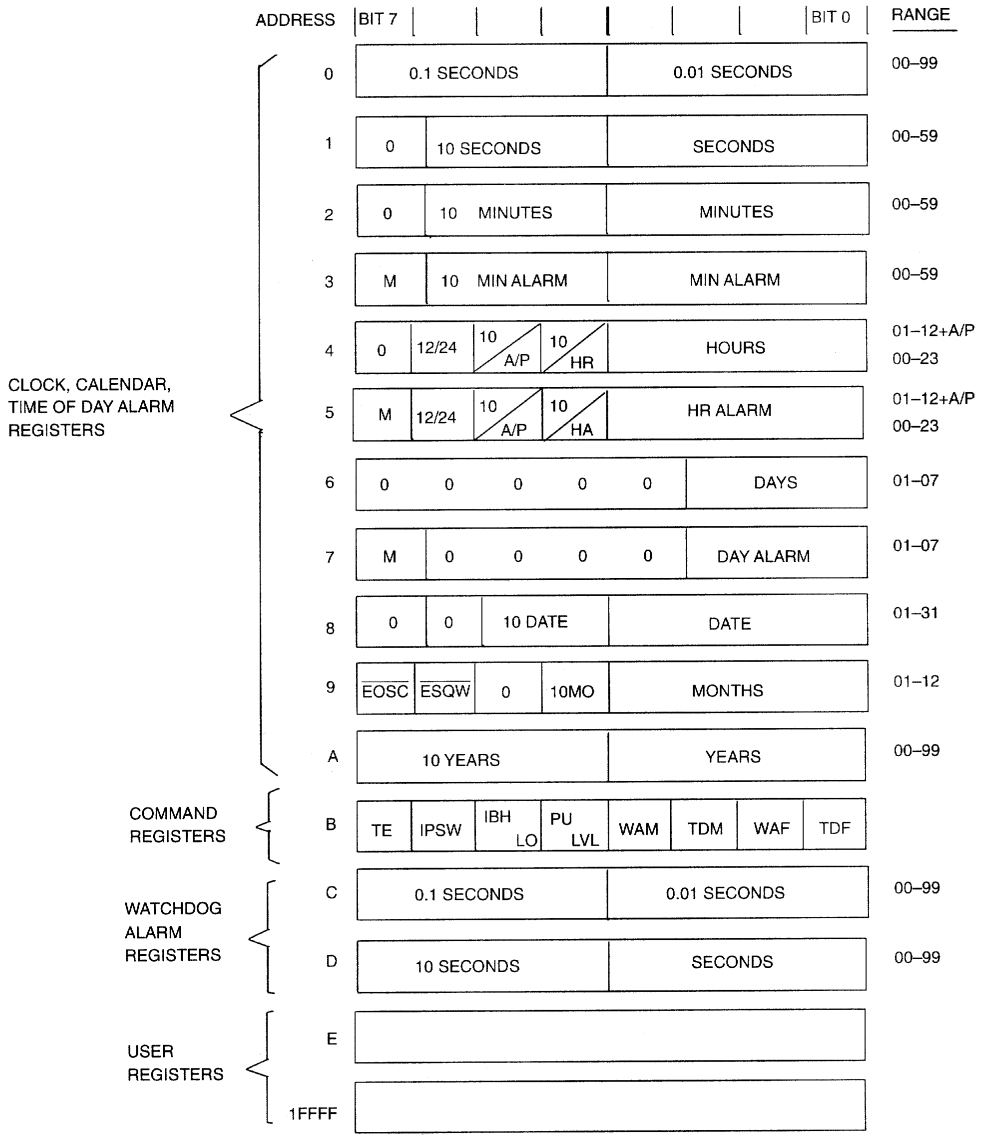
A key feature of the Dallas Watchdog Timekeepers is that two different interrupt outputs are provided: a time of day alarm and a watchdog interrupt. These two interrupts are controlled by the Command

Register, time of day alarm registers, and watchdog alarm registers. The Command Register allows flexibility in the operation of the interrupts. See Appendix for a complete description of the Command Register bits.

Time of Day Alarm

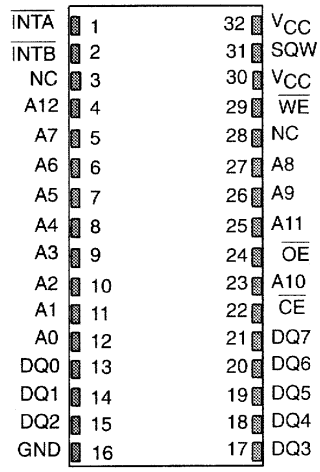
The first type of interrupt is the Time of Day Alarm. The Time of Day Alarm allows the user to program the device to generate an interrupt at a specific time of day for a specific day of the week. Special mask bits in the alarm registers also make it possible for this alarm to generate an interrupt once per minute, once per hour, or once per day.

DS1486 RAMIFIED TIMEKEEPER REGISTERS Figure 1



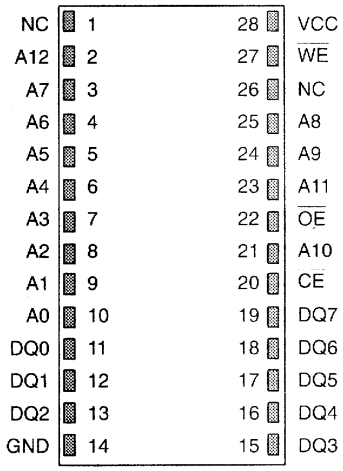
COMPARISON OF WATCHDOG TIMEKEEPER AND JEDEC BYTEWIDE PINOUTS Figure 2

WATCHDOG TIMEKEEPERS

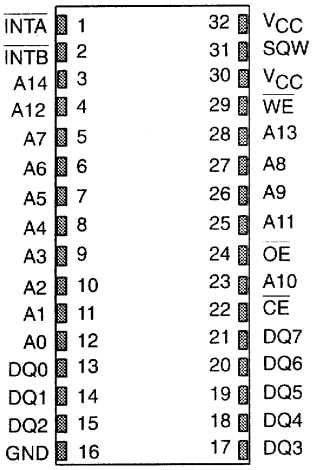


DS1386 8K X 8

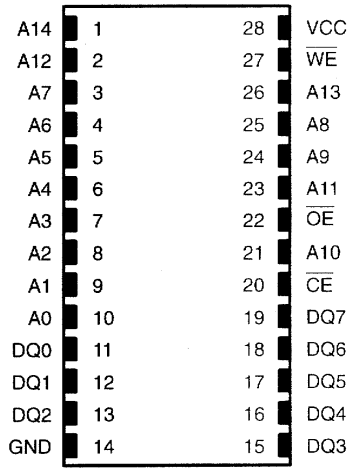
JEDEC BYTEWIDE



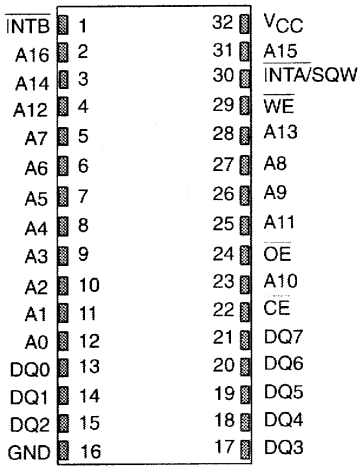
8K X 8 SRAM



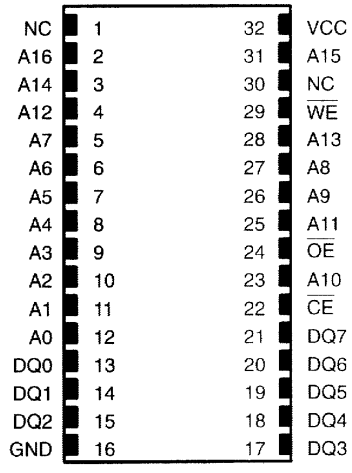
DS1386 32K X 8



32K X 8 SRAM



DS1486 128K X 8



128K X 8 SRAM

Watchdog Alarm

The second type of interrupt is the Watchdog Alarm. The Watchdog Alarm allows the user to program the device to generate a periodic interrupt at a user-defined interval. The user can program the device to generate an interrupt every 0.01 seconds to 100 seconds in 0.01-second increments. The watchdog interrupt is typically used in one of two different ways: as a microprocessor monitor or as a periodic interrupt.

Watchdog Alarm as Microprocessor Monitor

The Watchdog Alarm is often used as a microprocessor monitor in critical applications. In this function, the Watchdog Alarm is used to ensure that the microprocessor does not go out of control. For this type of application, the system is designed such that the microprocessor "checks in" with the Watchdog Timekeeper periodically by reading or writing to any of the watchdog alarm registers. Each time the microprocessor "checks in" with the Watchdog Timekeeper the watchdog timer is reset. If the microprocessor does not "check in" within the user specified watchdog interval, the Watchdog Alarm will generate an interrupt. This interrupt is used to reset the microprocessor. Figures 3 and 4 show two different ways that the Watchdog Timekeeper is interfaced with a microcontroller to monitor the system for an out of control condition.

In Figure 3, the interface between the DS1386–08 and the 68HC11 microcontroller is illustrated. In this diagram, $\overline{\text{INTA}}$ from the DS1386–08 is connected to the interrupt request (IRQ) pin of the 68HC11. In this example, the 68HC11 can be programmed such that it will reset the system if $\overline{\text{INTA}}$ is allowed to go active. Figure 4 illustrates the interface between the DS1386–08 and the 8051 microcontroller. In this example, the $\overline{\text{INTA}}$ pin is connected to one input of a 74LS122 one-shot circuit. The output of the one-shot is connected to the reset (RST) pin of the 8051. In this circuit, if the watchdog timer is allowed to time out, the $\overline{\text{INTA}}$ pin will go active, causing the one-shot to provide a pulse to the 8051 reset and thus reset the 8051.

It should be noted that in both examples the interrupt output was not connected directly to the microcontroller reset. The reason for this is related to one of the options that is provided in the Command Register. The Command Register allows the interrupts to be programmed to generate either a pulse or a constant level signal in the event that the interrupts are activated. When the pulse option is provided, there is no problem with connecting the $\overline{\text{INTA}}$ output directly to the reset pin. However, if the constant level signal mode is selected, the microcontroller would be permanently locked in reset since there would be no way to clear the interrupt (since the interrupt output would permanently hold the microcontroller in reset). With this in mind, connecting the interrupts directly to the reset input is never recommended. Even if the designer programs the interrupts to run in pulse mode, it is still possible that the level mode could be accidentally activated by a software error, which would cause the microcontroller to be permanently locked in reset.

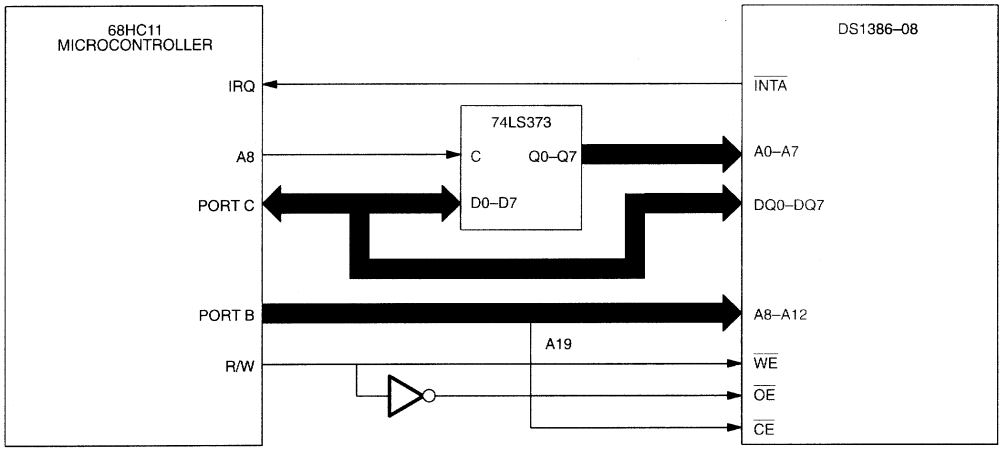
Watchdog as Periodic Interrupt

A second popular way that the Watchdog Alarm is used is as a periodic interrupt. In this case the Watchdog Timekeeper is programmed to generate an interrupt and, in contrast to the above example, the intention is to allow the interrupt to occur. In this example the device will generate an interrupt periodically at a user-defined interval. Using the interrupt in this manner is useful, for example, in data acquisition equipment. The interrupt is used to tell the system to collect data each time it is activated. The circuit illustrated in Figure 3 could be used for this type of application. In this example the microcontroller could be programmed to gather data whenever an interrupt is activated.

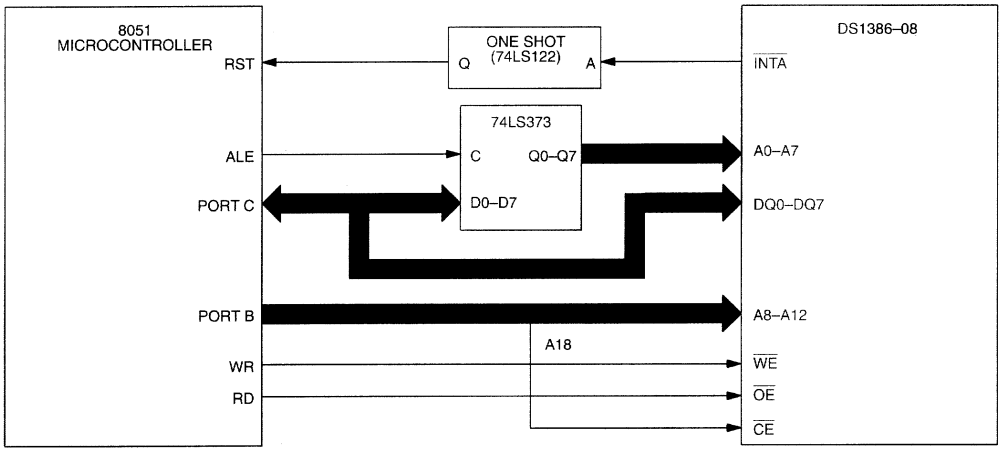
Interrupt as "Wake Up" Signal

One important feature of the interrupt outputs of the Watchdog Timekeeper is that they can be enabled even when system power is off and the device is in battery-backed operation. This is particularly useful in applications where the system is shut off to conserve power when not in use. Either of the two interrupts can be used to "wake up" a system or specific circuitry within a system. The specified task can be completed and then the system can be shut off again. The system will remain powered down until the Watchdog Timekeeper tells the system to power up again. It should be mentioned that the interrupt outputs must be selected for active low operation to function when in battery backed mode.

WATCHDOG TIMEKEEPER INTERFACED WITH 68HC11 MICROCONTROLLER Figure 3



WATCHDOG TIMEKEEPER INTERFACED WITH 8051 MICROCONTROLLER Figure 4



One important consideration when using an interrupt to "wake up" a system is to insure that no pins on the Watchdog Timekeeper are interfacing with any logic that is at a greater potential than the battery voltage when system power is turned off. If a pin is at a potential that is greater than the battery voltage when the system power is turned off, this will cause the positive ESD (electrostatic discharge) protection diode to forward bias. This allows current to flood the substrate of the Watchdog Timekeeper, which in turn can cause the oscillator to stop.

IDEAL APPLICATIONS

Dallas Watchdog Timekeepers are ideally suited for many different types of applications. In general, this product family is a perfect fit for any system that requires a real time clock, nonvolatile RAM, and interrupt capabilities. Furthermore, the upgrade path in RAM densities make this product even more attractive for designers who see the potential need for greater RAM densities. The near–JEDEC bytewide footprint and the easy software interface with the Watchdog Timekeeper further its appeal as a simple product to use.

The interrupt outputs provided by the Watchdog Timekeepers offer much flexibility to a designer. These interrupts can be used to signal a system to perform an event at a specific time and/or can be used in critical applications to monitor the microprocessor to insure that it does not run "out of control." Additionally, the interrupts can be operated even when the device is in battery backed operation. This allows the designer to use the Watchdog Timekeeper to "wake up" a system.

TROUBLESHOOTING

The Dallas Watchdog Timekeepers have proven to be highly reliable and meet the published specifications. However, during the course of development, some common difficulties could be experienced. This section is provided as a summary of the most common problems that could be encountered and gives the solution to those problems.

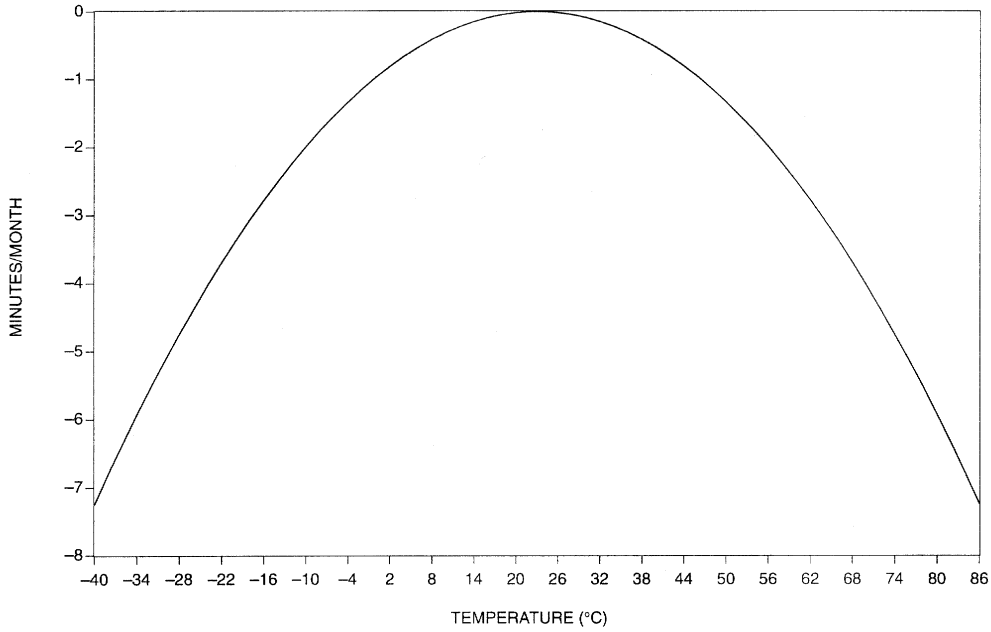
1. Clock is Inaccurate (i.e., greater than ±1 minute/ month at 25°C)

   It is possible to cause the Watchdog Timekeeper to run slow by periodically stopping the oscillator. This can be caused inadvertently by noisy input signals to the Watchdog Timekeeper. If an input signal rises to a voltage that is greater than a diode drop (~0.3 volts) above V_{CC}, the ESD protection diode for the input pin will forward bias allowing the substrate of the device to be flooded with current. This, in turn, can stop the oscillator until the input signal voltage decreases to below a diode drop above V_{DD}.

   There is a second scenario that can also cause the clock to appear to run slow. This scenario is similar to that above. If the Watchdog Timekeeper is in battery back–up mode, it is important to insure that none of the input signals is at a potential that is greater than the battery voltage. This needs to be considered especially for applications that use the interrupt signals when the Watchdog Timekeeper is in battery back–up operation. Since the interrupt outputs are open drain, they need to have external pull-up resistors. When the Watchdog Timekeeper is in battery back–up operation, it is necessary to insure that the interrupts are not pulled up to a potential that is greater than the battery voltage, otherwise the ESD protection diode will be forward biased, which can cause the oscillator to stop running.

   Also, it should be mentioned that the Watchdog Timekeepers will be most accurate when run at room temperature (25°C). Figure 5 illustrates the accuracy of a typical real time clock over temperature. As can be seen from the graph, timekeeping accuracy is temperature-dependent and becomes less accurate the further the ambient temperature deviates from +25°C.

REAL TIME CLOCK ACCURACY OVER TEMPERATURE Figure 5



2. Interrupts Do Not Work

   Several situations can cause this problem.

   a. The interrupt outputs are open drain. Therefore, $\overline{\text{INTA}}$ needs an external pull–up resistor and $\overline{\text{INTB}}$ (INTB) needs an external pull–up resistor when set for active low operation and needs an external pull–down resistor when set for active high operation. If the pull–up or pull–down resistors are not used, the interrupts will not function properly.

   b. When in battery back–up operation, only active low mode can be used for $\overline{\text{INTB}}$ (INTB). Active high mode for the $\overline{\text{INTB}}$ (INTB) pin will not function when the Watchdog Timekeeper is in battery back–up mode.

3. Cannot Write to Real Time Clock

   Insure that the TE (Transfer Enable) bit has been set to a logic 1. This allows data written in the outer buffers to be transferred into the real time clock registers.

4. Clock will not run

   Insure that the oscillator enable bit ($\overline{\text{EOSC}}$, bit 7 of register 9) is set to a logic 0.

5. Alarm Flags do not work

   Alarm flags are set only as long as the corresponding interrupt output is active. Therefore when the interrupts are set to operate in pulse mode, the alarm flag will be set only during the active pulse of the interrupt. If level mode operation is selected, the interrupt will remain until the alarm condition is cleared.

APPENDIX: COMMAND REGISTER

Address location 0Bh is the Command Register where mask bits, control bits and flag bits reside. The operation of each bit is as follows:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TE	IPSW	IBH/LO	PU/LVL	WAM	TDM	WAF	TDF

TE (Bit 7 Transfer enable) – This bit when set to a logic 0 will disable the transfer of data between internal and external clock registers. The contents in the external clock registers are now frozen and reads or writes will not be affected with updates. This bit must be set to a logic 1 to allow updates.

IPSW (Bit 6 Interrupt switch) – When set to a logic 1, $\overline{\text{INTA}}$ is the Time of Day Alarm and INTB/($\overline{\text{INTB}}$) is the Watchdog Alarm. When set to logic 0, this bit reverses the output pins. $\overline{\text{INTA}}$ is now the Watchdog Alarm output and INTB/($\overline{\text{INTB}}$) is the Time of Day Alarm output.

IBH/LO (Bit 5 Interrupt B Sink or Source Current) – When this bit is set to a logic 1 and V_{CC} is applied, INTB/($\overline{\text{INTB}}$) will source current (see DC characteristics I_{OH}). When this bit is set to a logic 0, INTB will sink current (see DC characteristics I_{OL}).

PU/LVL (Bit 4 Interrupt pulse mode or level mode) – This bit determines whether both interrupts will output a pulse or level signal. When set to a logic 0, $\overline{\text{INTA}}$ and INTB/($\overline{\text{INTB}}$) will be in the level mode. When this bit is set to a logic 1, the pulse mode is selected and $\overline{\text{INTA}}$ will sink current for a minimum of 3 ms and then release. INTB/($\overline{\text{INTB}}$) will either sink or source current, depending on the condition of bit 5, for a minimum of 3 ms and then release.

WAM (Bit 3 Watchdog Alarm Mask) **–** When this bit is set to a logic 0, the Watchdog Interrupt output will be activated. The activated state is determined by bits 1, 4, 5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Watchdog interrupt output is deactivated.

TDM (Bit 2 Time of Day Alarm Mask) – When this bit is set to a logic 0, the Time of Day Alarm Interrupt output will be activated. The activated state is determined by bits 0, 4, 5, and 6 of the COMMAND REGISTER. When this bit is set to a logic 1, the Time of Day Alarm interrupt output is deactivated.

WAF (Bit 1 Watchdog Alarm Flag) – This bit is set to a logic 1 when a watchdog alarm interrupt occurs. This bit is read only.

The bit is reset when any of the Watchdog Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.

TDF (Bit 0 Time of Day Flag) – This is a read-only bit. This bit is set to a logic 1 when a Time of Day alarm has occurred. The time the alarm occurred can be determined by reading the Time of Day Alarm registers. This bit is reset to a logic 0 state when any of the Time of Day Alarm registers are accessed.

When the interrupt is in the pulse mode (see bit 4 definition), this flag will be in the logic 1 state only during the time the interrupt is active.